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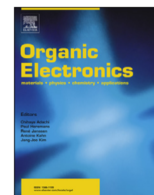

Low voltage and high frequency vertical organic field effect transistor based on rod-coating silver nanowires grid electrode

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We report on low voltage and high frequency vertical organic field-effect transistors (VOFETs) using silver nanowires (AgNWs) as intermediate grid electrode (source) deposited through Mayer rod-coating. The optimized AgNWs electrodes deposited on insulator surface followed by low thermal annealing have sheet resistance of ~30 Ω/sq and surface roughness of 70 ± 20 nm. Crosslinked poly(vinyl alcohol) is used as gate insulator and C_{60} fullerene as n-type channel semiconductor. Our VOFETs have high output current density of 2.5 mA/cm^2 and on/off ratio of 5×10^3 with supply voltages up to 2 V. A fast switching performance of sub-1 µs at frequency gate modulation of 0.13 MHz is demonstrated. Moreover, our devices are produced based on low-cost methods compatible with industrial-scale production of organic electronics.

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1. Introduction

Transparent conductive electrodes (TCEs) based on nanostructured materials attract considerable interest in optoelectronics due to the combination of low sheet resistance (R_{sh}), transparency and, in general, low processing costs [1]. In this way, several nanostructured materials such as carbon nanotubes, graphene, and metal nanowires were proposed as TCEs [2–4]. Among them, silver nanowires (AgNWs) are considered one of the most promising candidates due to their excellent electrical, mechanical, thermal and optical properties [5], especially as transparent electrodes in organic light-emitting diodes (OLEDs) and organic solar cells (OSCs) [6–8]. Moreover, they are also interesting for electronic devices where transparency to visible light is not fundamental, as is the case of intermediate electrodes in Vertical Organic Field Effect Transistors (VOFETs).

A VOFET is essentially a semiconductor diode stacked over a capacitor separated by a common intermediate electrode usually acting as source [9]. The device is governed by the source-semiconductor interface where the gate bias modulates the carrier density within the semiconductor due to the electrical field transparency of the intermediate electrode. Such transparency must arise without significant increase in the in-plane resistivity to ensure homogenous potential along the device [10].

Many different materials have been considered as intermediate electrodes in VOFETs, for example, ultra-thin evaporated metallic films are commonly used [9,11], but at low voltages, considerable shielding effects are observed, while source electrodes with random carbon nanotubes have demonstrated great electric permeability to the electric field but considerable high R_{sh} (>kΩ/sq) [12]. Other alternatives using graphene either in horizontal or vertical heterostructures [13–15], block-copolymer templates [16], ultra-thin ITO films [17], and atomic layer deposition assisted nanoimprint lithography [18] have provided excellent performances, but their relatively high costs are not totally compatible with the potential advantages of the low production costs of VOFETs. Recently, thermally evaporated Sn thin films under controlled conditions were used and presented good performances at low voltages, however with low on/off ratios [10]. Metallic nanowires (Ag/Au) were used as intermediate electrode in the past with on/off ratios of ~10^5 at considerable high voltages [19], however, the method used based on solution-processed nanowires can be incompatible with common organic insulators.

To overcome these obstacles, in this work we report on a VOFET using AgNWs as intermediate grid electrode deposited through Mayer rod-coating, a simple and low-cost thin film deposition method.

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2. Experimental details

VOFETs were prepared depositing 80 nm thick Al as gate electrode by thermal evaporation at 8×10^{-6} torr on previously cleaned glass substrates. The gate insulator was prepared based on previous work [20]. Poly(vinyl alcohol), PVA, purchased from Sigma-Aldrich (130 kDa) was used without further purification and dissolved in ultra-pure deionized water (18.2 MΩ cm) at concentration of 60 mg/ml. The PVA solution was then kept under stirring for 1 h at 60 °C. In the sequence, ammonium dichromate (AD) from Synth-Brazil (99.5%) was added to the PVA solution at 25% w/w and filtered using 0.22 μm pore filters (Merck Millipore). Then, the AD:PVA solution was deposited on the gate surface by spin coating at 3000 rpm during 60 s, followed by 12 min of UV treatment (365 nm, 8 W) resulting in ~350 nm thick crosslinked PVA (cr-PVA) film. Next, the cr-PVA thin film was annealed at 110 °C in an oven for 1 h. As intermediate electrode, AgNWs from ACS Material (MA, USA) with ~99.5% purity, 40 nm of diameter and length of about 20–30 μm was diluted in isopropyl alcohol (IPA) to form a suspension of 5 mg/ml. The grid electrode was deposited on cr-PVA surface of 2.5 cm × 1.5 cm area using a wire-wound rod (Mayer rod)-coating # 10 purchased from R. D. Specialties (NY, USA). For each of the 4 layers in our devices, 40 μL of AgNWs suspension was used. An interval of 5 min was taken between each AgNWs layer to assure IPA evaporation. After all AgNWs layers were deposited, the sample was annealed during 40 min on a hot plate in air at 120 °C to remove the oxidation layer and increase the contact between AgNWs junctions [21]. Then, ~120 nm of C_{60} fullerene (n-type semiconductor) from Sigma-Aldrich was deposited by thermal

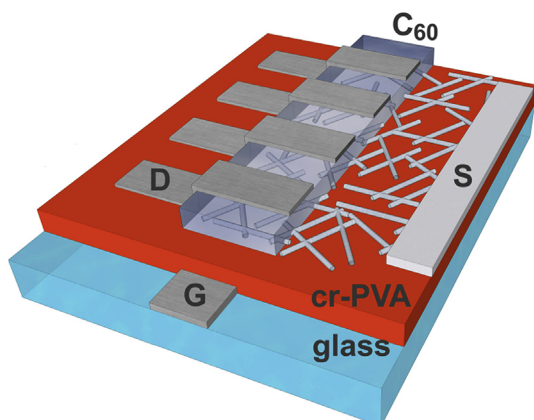

Fig. 1. 3D illustration of the Al/cr-PVA/AgNWs/C_{60}/Al VOFET with AgNWs intermediate grid electrode acting as source.

Fig. 2. 4 layers of AgNWs deposited using wire-wound rod (Mayer rod)-coating # 10 on cr-PVA surface: (a) R_{sh} *vs* annealing time at 120 °C. The quality of the fitting using an exponential decay is 0.99789 (chi-square); (b) SEM image for AgNWs after 40 min of annealing at 120 °C; (c) pristine AgNWs; (d) SEM image for larger area of AgNWs annealed; (e) surface cross-section along the line shown in f; (f) 3D confocal topography for AgNWs annealed for 85 μm × 85 μm area; (g) resistance measured at the edges of 2.5 cm × 2.5 cm AgNWs electrode after annealing, lateral contacts were made with silver paint. Same annealing in b was used for d, e, f, and g.

evaporation at 8 × 10^{-6} torr with a deposition rate of ~0.5 nm/s. Finally, as drain electrode, an 80 nm thick Al electrode was evaporated resulting in VOFETs with gate and drain overlap of 4 mm^2. Fig. 1 shows the final device structure.

Silver nanowires grid electrodes were morphologically characterized using confocal (Leica DCM 3D) and FEG-SEM (Jeol 7500F) microscopes. Sheet resistance was measured using the four-point van der Pauw method with a source-measurement unit Keithley 2400C. PVA and cr-PVA were characterized using thermogravimetric analysis (Netzsch STA 449F3). FT-IR spectra of PVA and cr-PVA thin films were obtained using a Bruker Vertex 70 spectrometer in ATR mode.

The transistor's electrical characterization was carried out at room temperature in air. Output and transfer curves were obtained using a source-measurement unit Keithley 2400C (D-S electrodes) coupled with an electrometer Keithley 6517A (S-G electrodes). Frequency response measurements were performed using the circuit shown in Fig. S1. An Autolab PGSTAT302 equipped with a FRA32M module was used for impedance spectroscopy. We fabricated and characterized 12 transistors and 8 of them exhibited equivalent performances, presented in this work.

3. Results and discussion

As discussed before, the intermediate electrode is key to the good performance of the VOFET, electrical transparency must be high without significant increase in R_{sh}. As deposited R_{sh} for different AgNWs layers are presented in Table S1 (Supplementary data). In order to obtain low R_{sh}, the films were annealed on a hot plate in air. The annealing temperature of 120 °C was chosen considering the thermal stability of the dielectric layer, Fig. S2. R_{sh} as a function of the annealing time and number of AgNWs layers are presented in Fig. 2 and Fig. S3 respectively.

As can be seen in Fig. 2, 4 layers is a good compromise between random meshes and conductivity. Fig. 2 (a) shows that R_{sh} of as-deposited AgNWs is about 114.7 ± 1.4 Ω/sq, but after 40 min at 120 °C this value decreases more than 70% to 28.2 ± 1.5 Ω/sq. The increase in conductivity after annealing is attributed to the better contact and partial fusion between the nanowires [21], confirmed by SEM images shown in Fig. 2 (b) when compared with pristine AgNWs (without annealing), Fig. 2 (c). Moreover, using ImageJ software in Fig. 2 (b) we found that 30% of cr-PVA surface area is covered by AgNWs. This covering is heterogeneous as seen in Fig. 2 (d), with holes between 2 and 5 μm.

After the optimized annealing is performed (120 °C during 40 min), the surface roughness root mean square (rms) is 70 ± 20 nm as can be seen in Fig. 2 (e) and (f), while the resistance of a 2.5 cm × 2.5 cm AgNWs electrode on cr-PVA is 22.4 Ω, Fig. 2 (g). Our morphological analyses indicate a fill factor (FF) of ~0.70 for the AgNWs electrodes considering the optimized parameters (number of AgNWs layers and annealing). Note that this high FF value was obtained keeping a high lateral conductivity, which is not commonly observed for other conventional intermediate electrodes in VOFETs [9–11,17]. Furthermore, considering the VOFET design rules from Ref. [22], the distance between the nanowires reported corresponds to the diameter (D) of the holes in the electrode while the rms value corresponds to the height (h), leading to an aspect ratio h/D low enough for high on/off ratios.

VOFETs were fabricated using the optimized AgNWs intermediate electrode. The device electrical response is presented in Fig. 3. In the polarization condition used the intermediate electrode (AgNWs) acts as electron source and the top electrode (Al) as electron drain. Output characteristics (J_{DS}-V_{DS}) for positively biased gate (V_{GS}) are shown in Fig. 3 (a). As can be seen J_{DS} increases as V_{DS} and V_{GS} are increased. The threshold voltage (V_T) as shown in Fig. 3 (b) is found to be 1.06 V. From Fig. 3 (c) the channel current density in the on-state (V_{GS} = 2 V) is about 2.5 × 10^{-3} A/cm^2 while the channel current density in the off-state (V_{GS} = 0 V) is about 5.0 × 10^{-7} A/cm^2 resulting in an on/off ratio of 5 × 10^3.

The leakage current density is similar to the channel current density found in the off-state (V_{GS} = 0 V). Nevertheless, the use of cr-PVA as dielectric has advantages, such as a low production cost and low capacitance [11,20]. Since the parasitic capacitance can be reduced, the low gate capacitance acts as a complementary factor to other two requirements for high switching frequencies in field-effect transistors: efficient charge transport in the semiconductor and small channel length [23]. The main source of parasitic capacitance expected in VOFETs is from gate-source overlap that

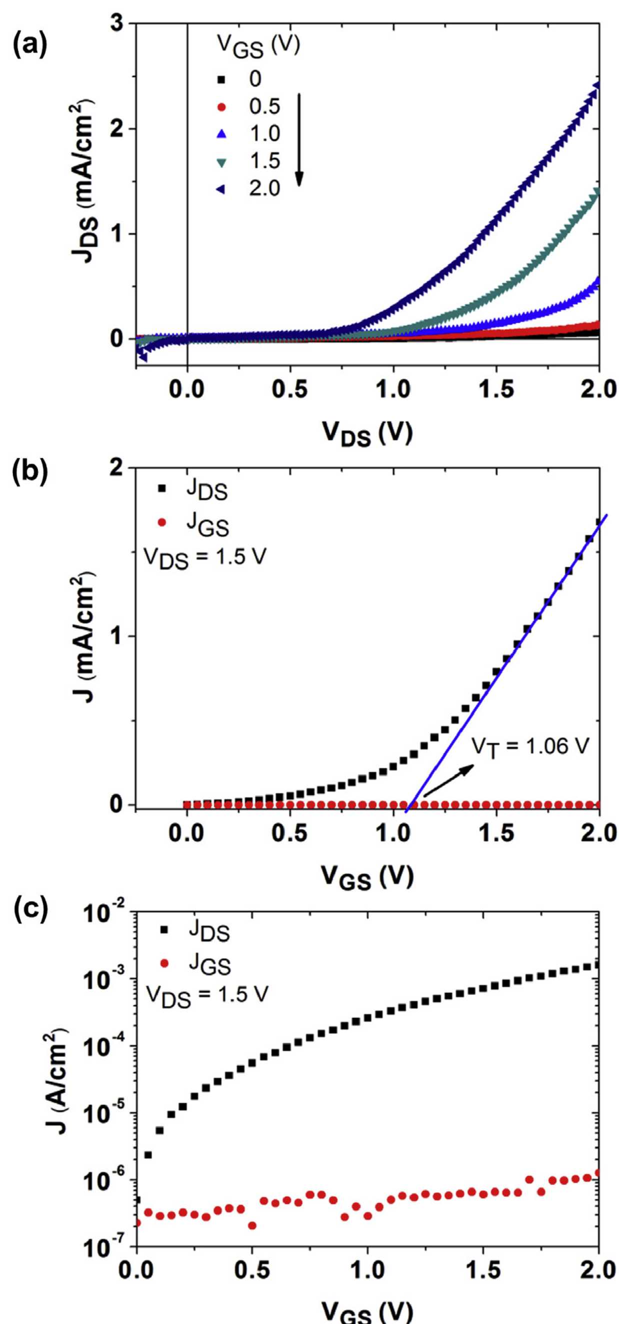

Fig. 3. (a) Output characteristics; (b) transfer characteristics (V_{DS} = 1.5 V) in linear and (c) monolog plots of the Al/cr-PVA/AgNWs/C_{60}/Al VOFET. V_T is the threshold voltage.

does not contribute to drain current [15]. VOFETs have a main advantage, the small channel length determined by the semiconductor thickness, opening the possibility for a fast switching performance as will be shown. The combination of ultra-short channel length and high electric fields leads to remarkable current densities under low supply voltages, as seen in Fig. 3.

The exponential dependence of J_{DS} on V_{GS} observed in Fig. 3 (a) is an evidence of the total current being limited by interface processes, possibly as a consequence of the potential barrier between the source electrode and semiconductor layer [10]. When the device is in the off-state, the injection barrier between AgNWs and C_{60} is approximately 0.4 eV [24], in this case charges are extracted from the active layer only due to the applied drain-source voltage presenting similarity to a diode structure where contact limited (CL) regime is expected [22], as shown in Fig. 4 (a). With the device in the on-state, negative charges are accumulated in the voids of the source electrode (AgNWs) creating a virtual contact that induces positive charges in the C_{60} close to AgNWs interface [22] decreasing the electron injection barrier from the AgNWs to C_{60}.

In this configuration, the channel current can be affected by the gate bias where the device behaves according to space charge limited current (SCLC) [22,25]. Under SCLC regime, the channel current follows the Mott-Gurney law where $J_{on} \propto V_{DS}^2$ [22,25,26], as shown in Fig. S4. The scaling exponent of 2.5 obtained in Fig. S4 can be associated to electron traps within the semiconductor that influence the SCLC regime due to the Poole-Frenkel effect [26], Fig. 4 (b) process I. However, if the gate-source voltage is not high enough to create an ohmic contact at the interface, charges can be also injected by Fowler-Nordheim tunneling [27], Fig. 4 (b) process II.

In addition to electron traps within semiconductor, in fact the main charge traps in our devices are probably from hydroxyl and ketone groups in the cr-PVA layer [20]. These groups were known to act as electron traps, especially the ketone groups [28]. The PVA molecular structure is basically composed by carbon chains with large amounts of hydroxyl end groups. The crosslinking induced by ammonium dichromate is based on the interaction of the chromium ions with the PVA molecular structure that results in carbon double bonds, responsible for the increased resistivity of the dielectric. This reaction as observed from FT-IR spectra shown in Fig. S5 also produces ketones groups from the oxidation of the hydroxyl groups [29].

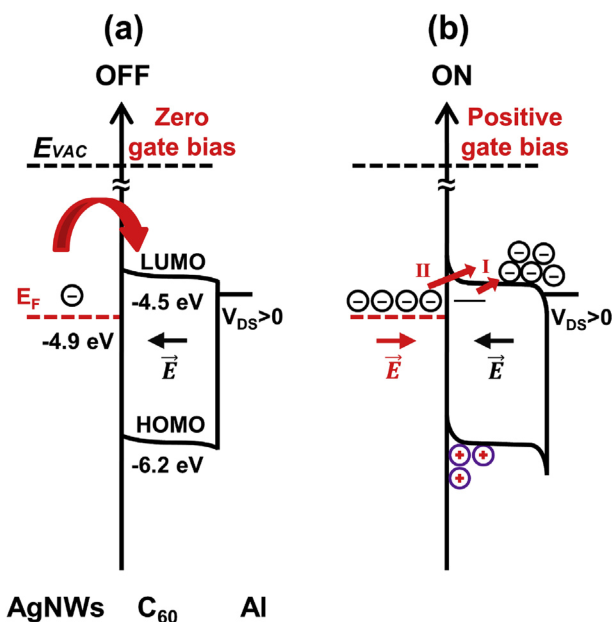

Fig. 4. Schematic energy diagram of AgNWs/C_{60}/Al interfaces, for: (a) zero gate bias; (b) positive gate bias.

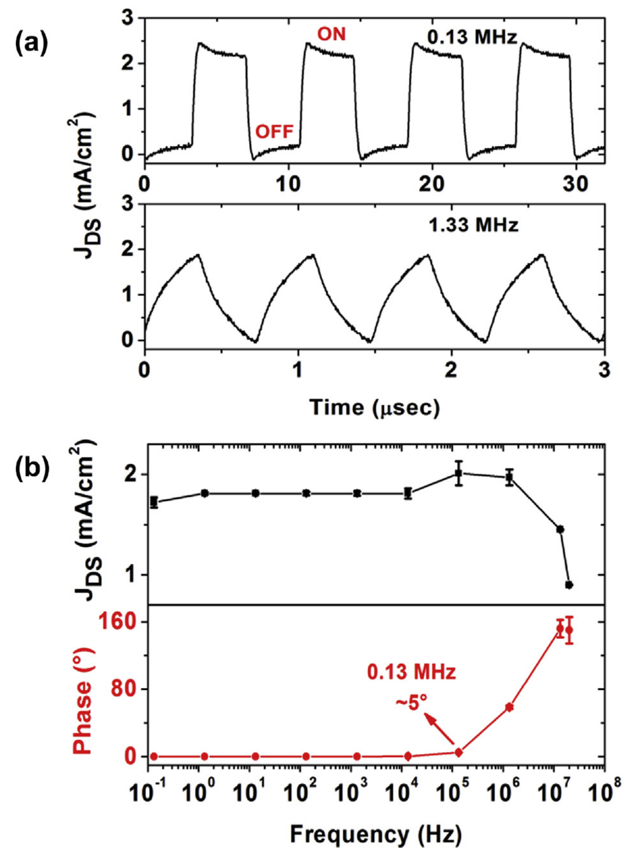

Fig. 5. Dynamic response of the Al/cr-PVA/AgNWs/C_{60}/Al VOFET: (a) 0.13 MHz and 1.33 MHz frequencies gate modulation; (b) modulated channel current density and phase in the on-state as a function of input frequency.

Fig. 5 shows the dynamic response of the VOFET to a square-wave input signal applied in the gate electrode with amplitude of 1.5 V and offset 0.75 V at different frequencies. V_{DS} was fixed at a DC voltage of 1.5 V. As can be seen in Fig. 5 (a), at frequencies up to 0.13 MHz the modulated channel current density follows the input square-wave signal. From fitting procedures, the response time under this modulation is $\tau_{rise}^{out} = 0.45$ μs and $\tau_{fall}^{out} = 0.55$ μs. Increasing the frequency to 1.33 MHz, the device current density

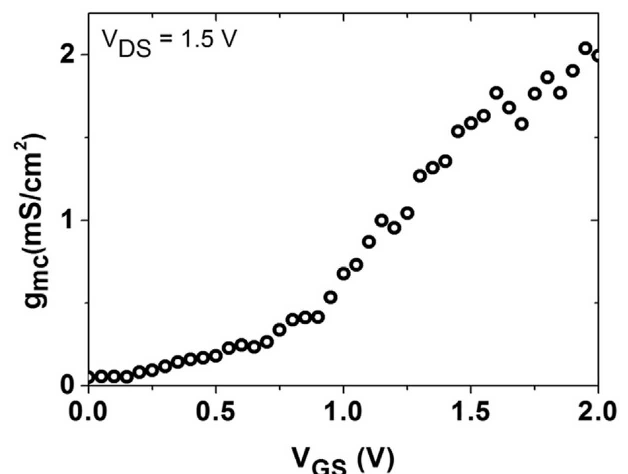

Fig. 6. Specific transconductance of the Al/cr-PVA/AgNWs/C_{60}/Al VOFET at $V_{DS} = 1.5$ V.

Table 1
Main VOFET characteristics of selected recent literature. On-current (I_{ON}) and specific gate capacitance (C_G) are presented by unit of area. I_{ON} is the highest current with device at on-state.

Intermediate electrode	Method	Active layer	I_{ON} (mA/cm^2)	C_G (nF/cm^2)	On/off	Ref.
Sn	Thermal evaporation	CuPc	0.175	[a]	[a]	[10]
Al	Thermal evaporation	C_{60}	0.013	27	$<10^2$	[11]
CNTs	Vacuum filtration	DNTT	110	354	$>10^4$	[12]
Graphene	CVD	P3HT	3400	~210	$>10^3$	[15]
ITO	Sputtering	ITO	~8	~7000	$\sim 10^5$	[17]
Ag/Au NWs	Self-assembly	N2200	>1	[a]	$\sim 10^5$	[19]
Au	Block-copolymer	N2200	~10	[a]	10^3	[32]
AgNWs	Mayer rod-coating	C_{60}	2.5	5	5×10^3	This work

[a] Not specified in the original work.

does not follow the input modulation anymore. In Fig. 5 (b) the modulated channel current density and its phase as a function of the input frequency is presented. Up to 0.13 MHz the modulated channel current density is basically the same whereas the phase starts to change from 0° to ~5°, which is still acceptable for electronic circuit application. However, for higher frequencies the modulated current decreases and there is a clear change in the phase showing that our devices have a switching limitation of about 10^5 Hz.

The switching speed of the transistor and its limitations shown in Fig. 5 are mainly related to the gate capacitance. As can be seen in Fig. S6 (a), the specific gate capacitance measured by impedance spectroscopy is between 2 and 5 nF/cm^2. However, for frequencies higher than 10^5 Hz the specific gate capacitance decreases significantly and the switching performance of the transistor starts to be limited by the sheet resistance of the intermediate electrode. Considering an ideal field-effect transistor, the maximum frequency of operation (where $I_{DS} = I_{GS}$) is defined by a large transconductance and low gate capacitance, $f_T = g_m/(2\pi C_G)$ [23]. In our case, the specific transconductance ($g_{mc} \equiv g_m$/area) at V_{GS} and V_{DS} of 1.5 V is ~1.5 mS/cm^2, as shown in Fig. 6. Assuming the specific gate capacitance of 5 nF/cm^2 at 1 Hz and the specific transconductance of 1.5 mS/cm^2, we project a cut-off frequency of ~50 kHz, close to the frequency where the phase starts to increase in Fig. 5 (b).

The frequency response of our devices could be improved even further by reducing the parasitic gate capacitance or using oxide dielectrics with ultra-low gate capacitance (<10 pF) [30]. However, oxides are not compatible with a full organic electronics perspective. On the other hand, hybrid dielectrics (organic-inorganic) are promising candidates [31].

Our VOFET based on the optimized AgNWs intermediate electrode using Mayer rod-coating presented performance comparable with those published so far in the recent literature, as can be seen in Table 1. The channel current has a better modulation compared to previous VOFET with similar materials but with ultra-thin (~20 nm) Al evaporated film as intermediate electrode [11]. While our device exhibited an on/off ratio of 5×10^3 the VOFET reported by Rossi et al. shows on/off ratios $<10^2$. The reason may be related to the porous nature of the AgNWs electrodes and thus higher FF and better electric field permeation.

In addition, our VOFET showed a sub-1 μs switching at low voltages opening possibilities for industrial circuit applications, for example, as drivers of active matrix OLED pixels [33]. Furthermore, the Mayer rod-coating deposition method presents wide compatibility with industrial-scale production at low-cost and can be also used in flexible substrates with low processing temperatures.

4. Conclusion

In summary, in this work we demonstrated an easy to prepare low-cost VOFET with silver nanowires as intermediate grid electrodes. We systematically investigated the deposition parameters of the AgNWs grid using Mayer rod-coating method. Applying the optimized parameters a VOFET was produced and characterized. The device exhibits a good performance with a high output density of 2.5 mA/cm^2 and on/off ratio of 5×10^3 with supply voltages up to 2 V. Moreover, this device presented a threshold voltage of about 1 V and a good switching performance up to 0.13 MHz.

Acknowledgments

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Appendix A. Supplementary data

Supplementary data related to this article can be found at http://dx.doi.org/10.1016/j.orgel.2017.08.011.

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